

B450 GAMING X																	
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B450 GAMING X

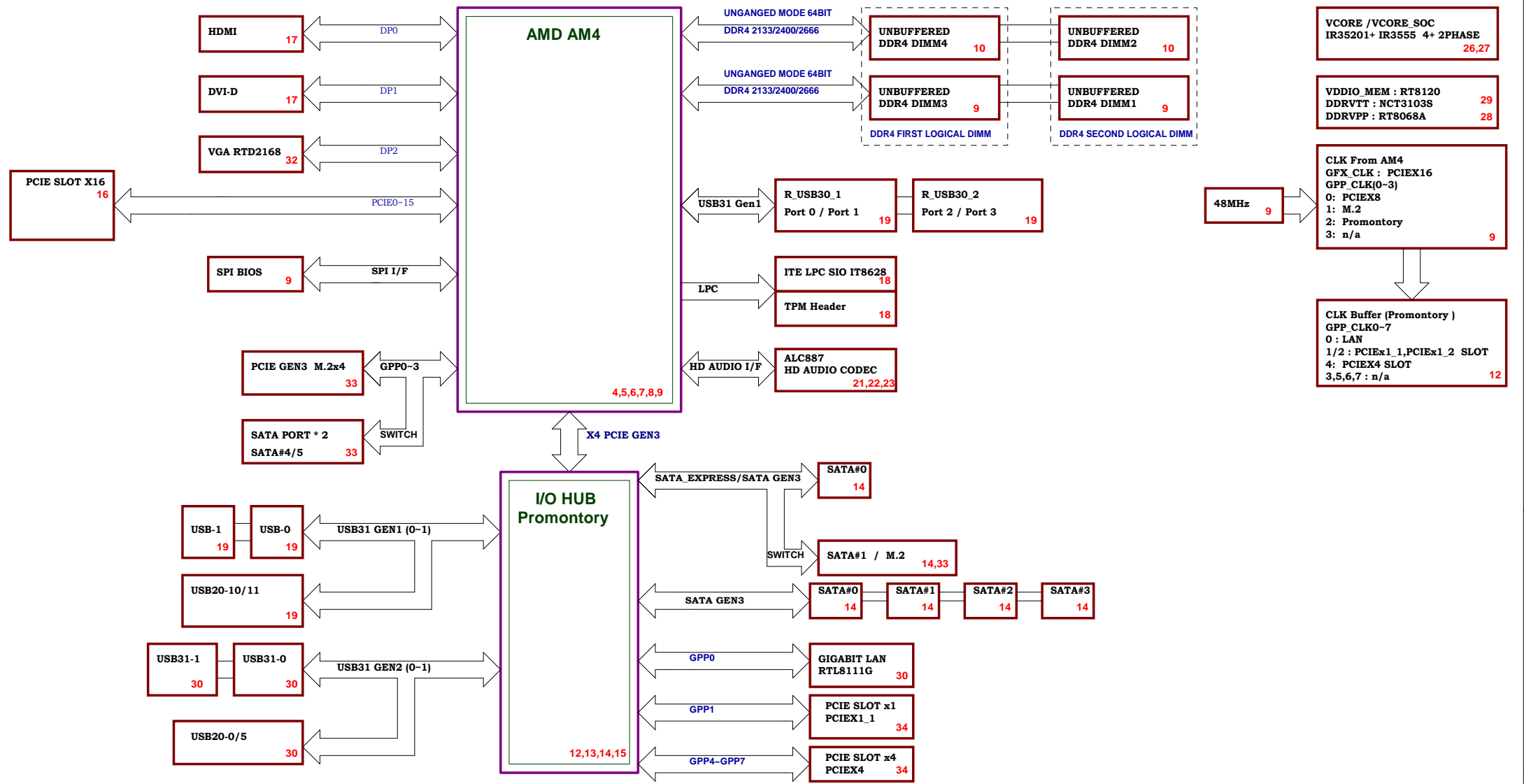
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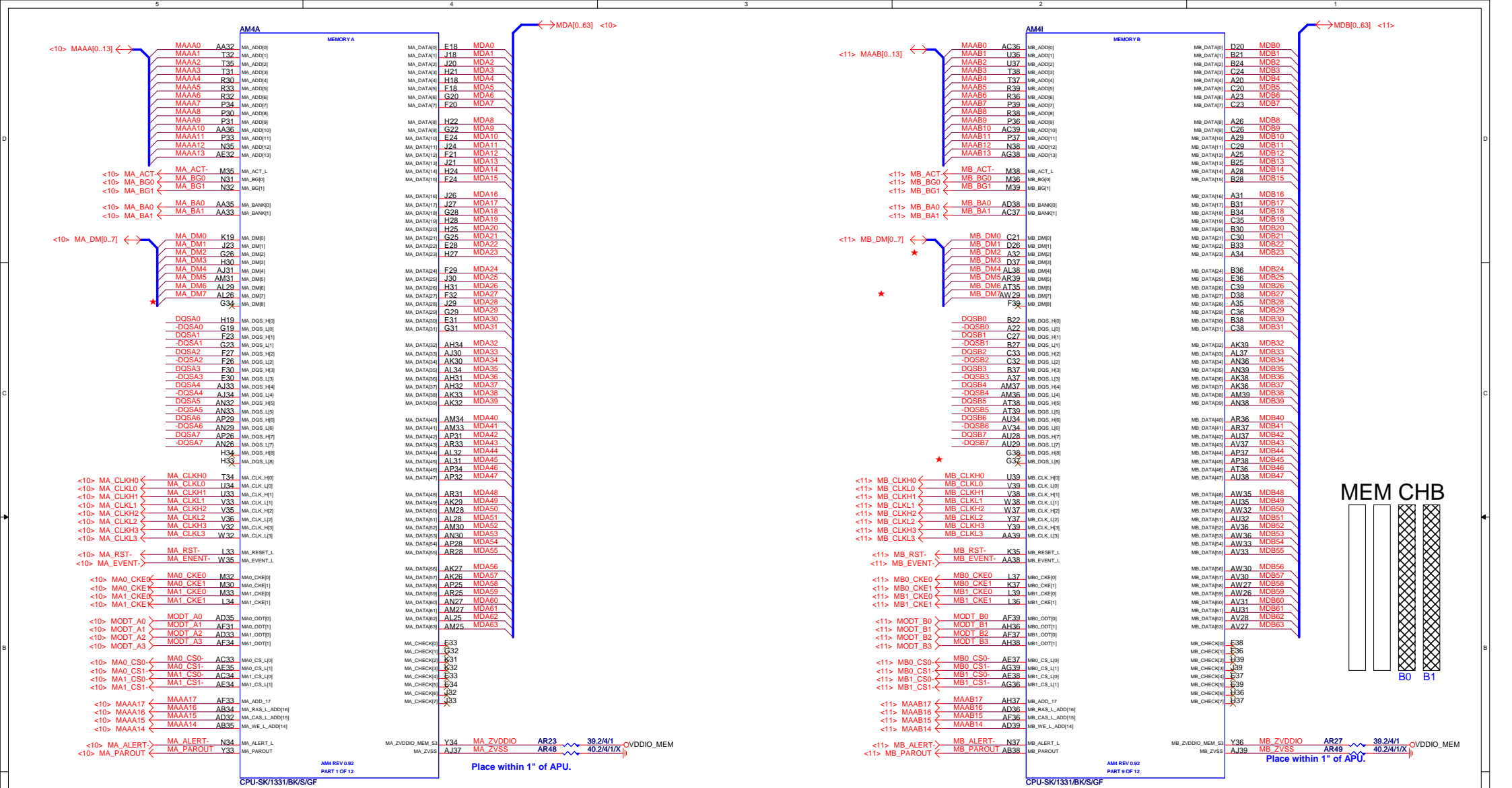
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B450 GAMING X

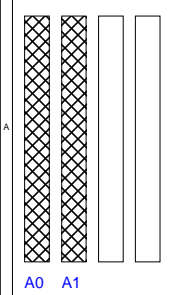
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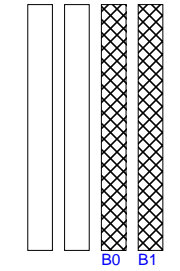




MEM CHA



MEM CHB



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Title: **APU DDR4**

Size: **Custom**

Document Number: **B450 GAMING X**

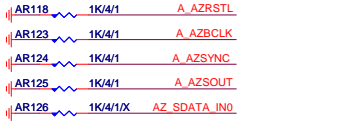
Rev: **1.0**

Date: **Monday, March 04, 2019**

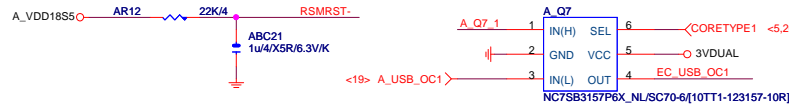
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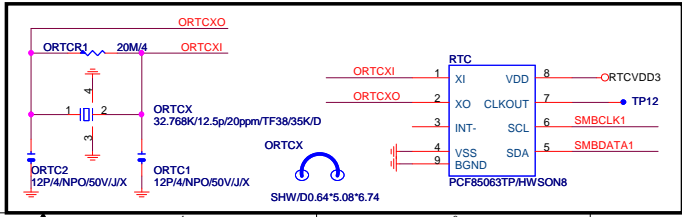
TEST0	TEST1	TEST2	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserve
0	1	X	Reserve
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on JTAG only, Yuba JTAG enable.



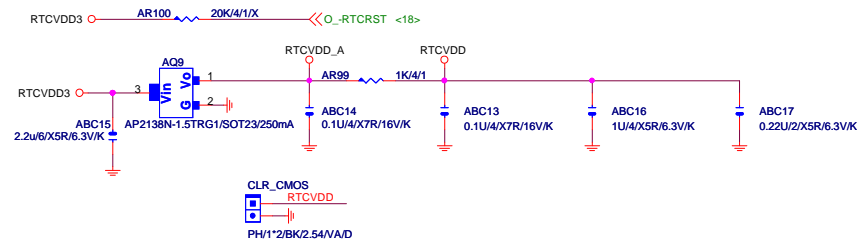
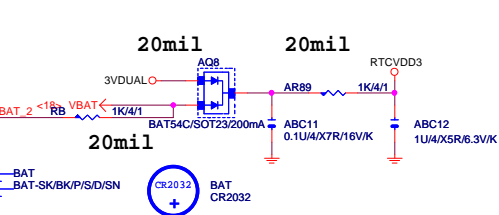
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	LPC_CLK0	LPC_CLK1	AGPIO3	RTC_CLK	LFRAME_L	SYS_RST#	SPI_CLK (ZP)
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48MHz crystal clock and generate both internal and external clocks (DEFAULT)	Enhanced reset logic (for quicker S5 S5 resume) (DEFAULT)	Coin battery is on board. (DEFAULT)	SPI ROM (DEFAULT)	normal reset mode (DEFAULT)	Use 48MHz crystal clock and generate both internal and external clocks (DEFAULT)
PULL LOW	BOOT FAIL TIMER DISABLED (DEFAULT)	Use 100MHz PCIE clock as reference clock and generate internal clocks only	Default to traditional reset logic	Coin battery is not on board.	LPC ROM	short reset mode	Use 100MHz PCIE clock as reference clock and generate internal clocks only
	C3/ST DIE ONLY						ZP DIE ONLY



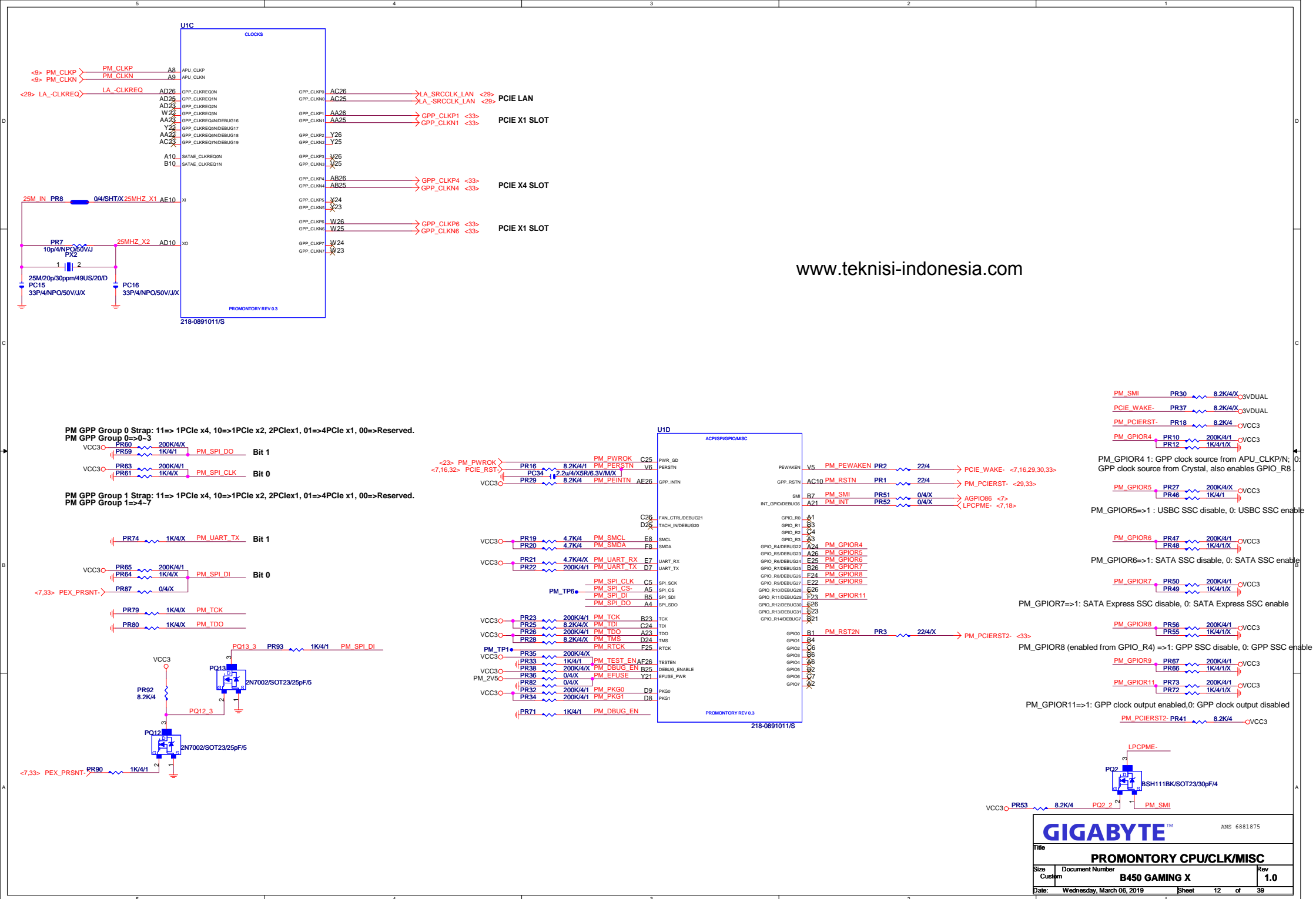
GIGABYTE™			
AM4 MISC			
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CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD P



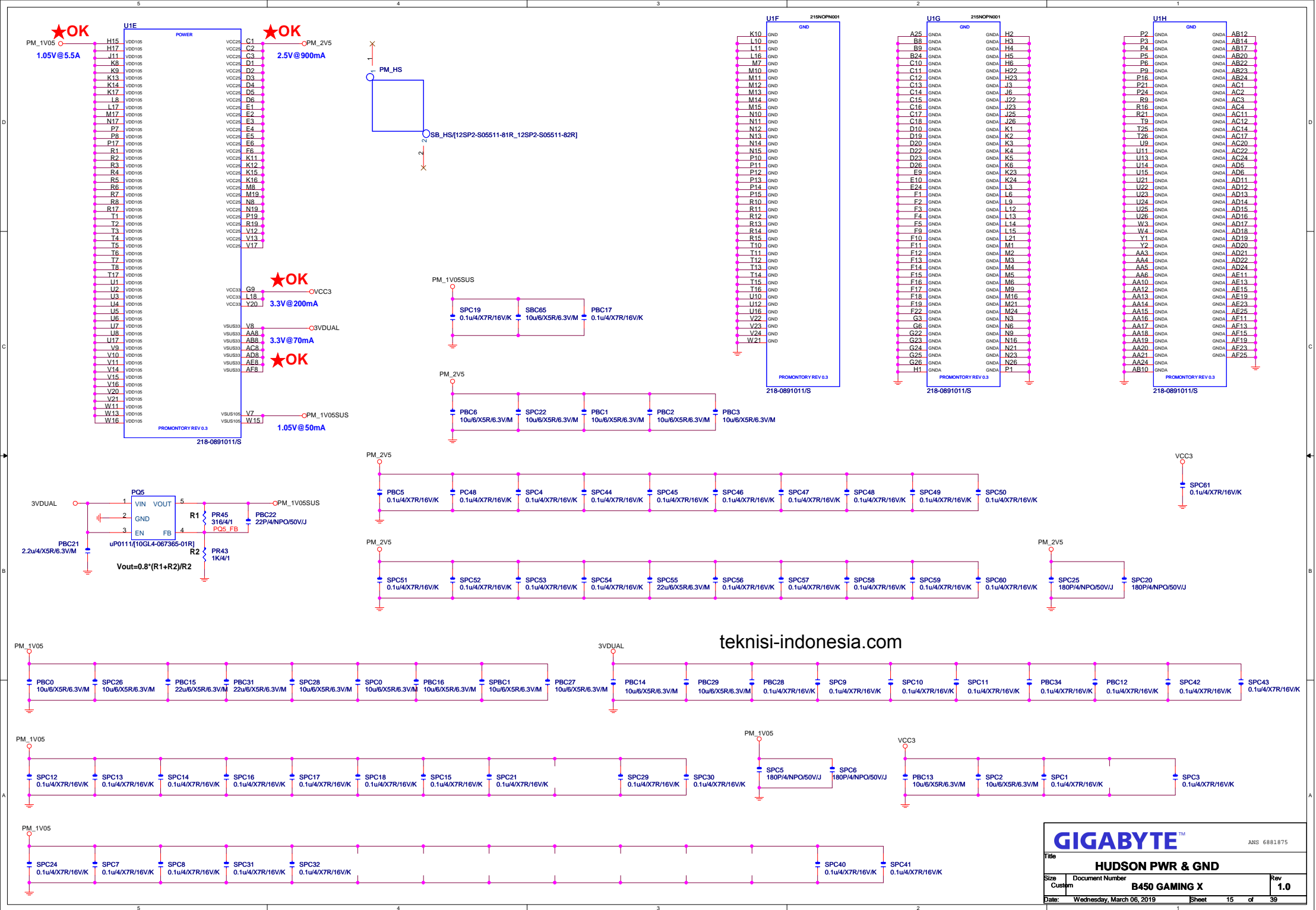


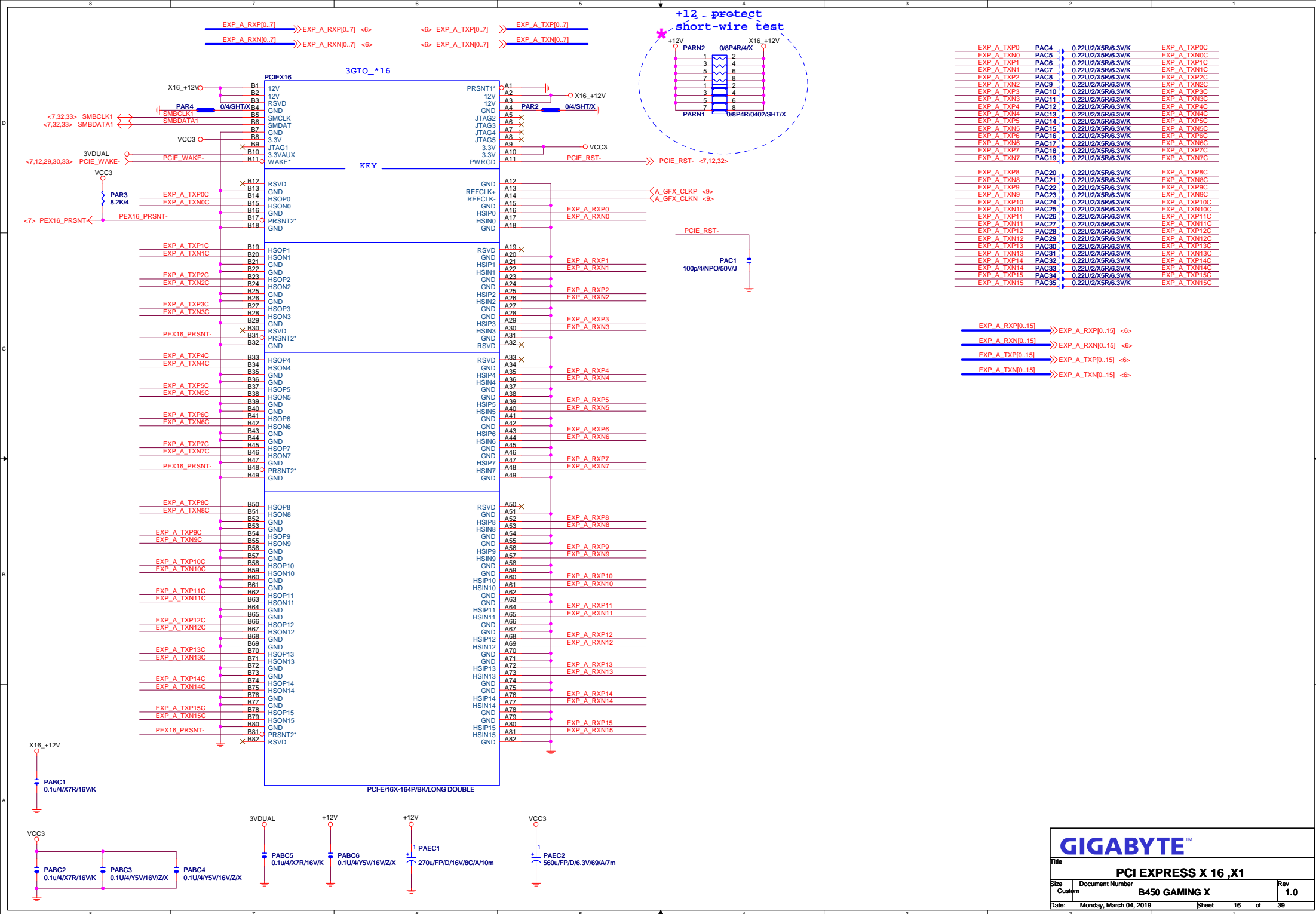


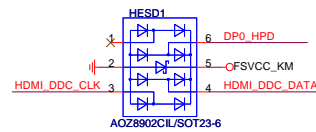
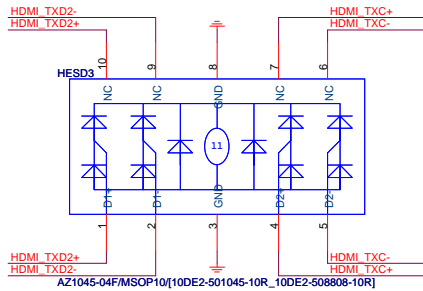
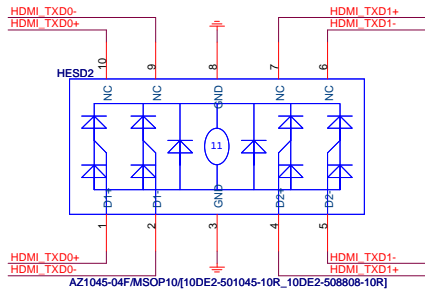
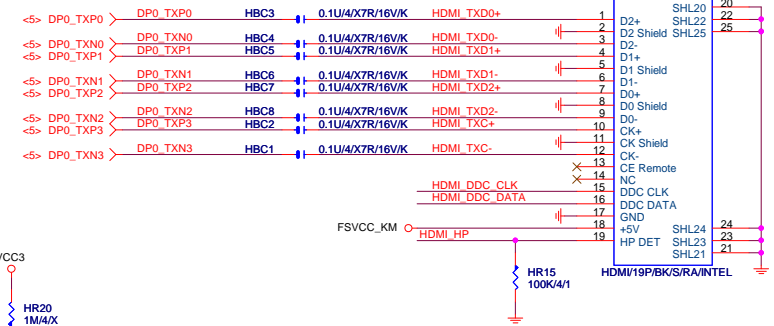
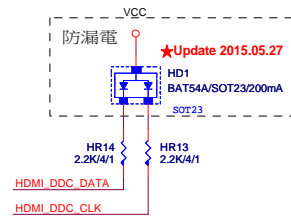
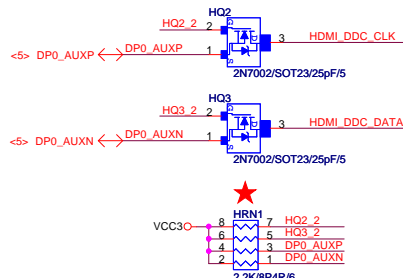
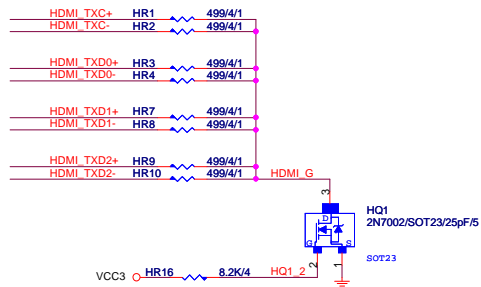
1

2

1



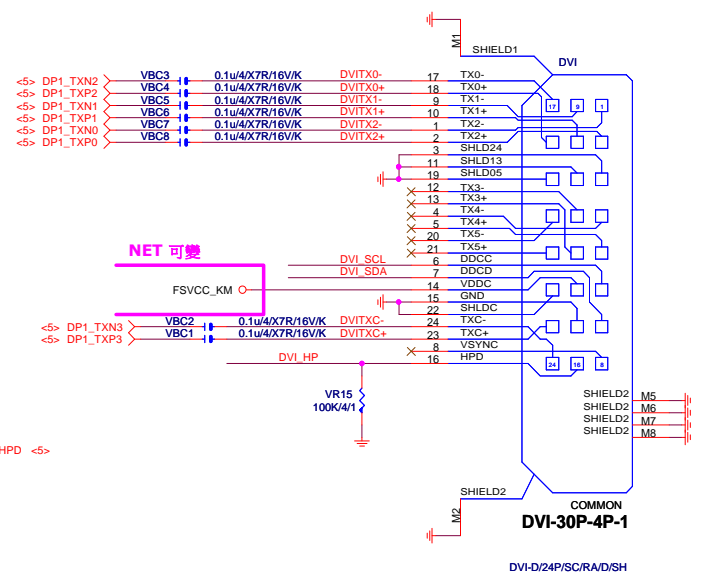
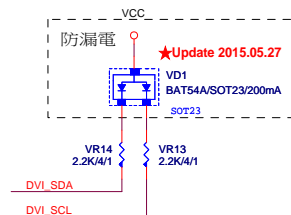
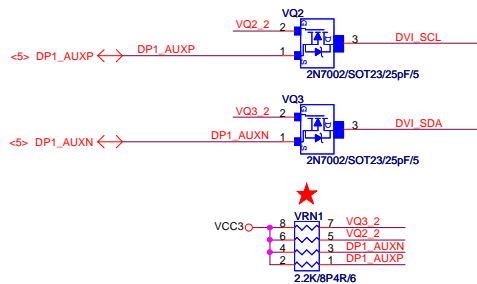
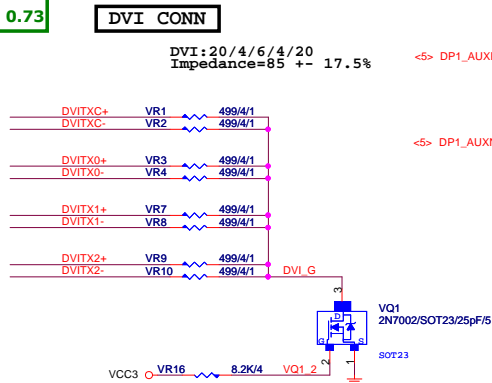




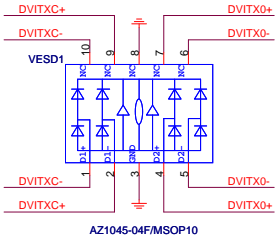
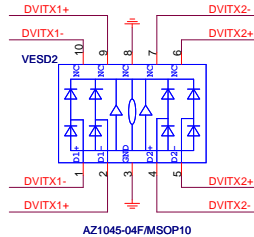
Rev: 0.73

DVI CONN

DVI: 20/4/6/4/20
Impedance=85 +/- 17.5%



Close to connector



NET 可變

Close to connector

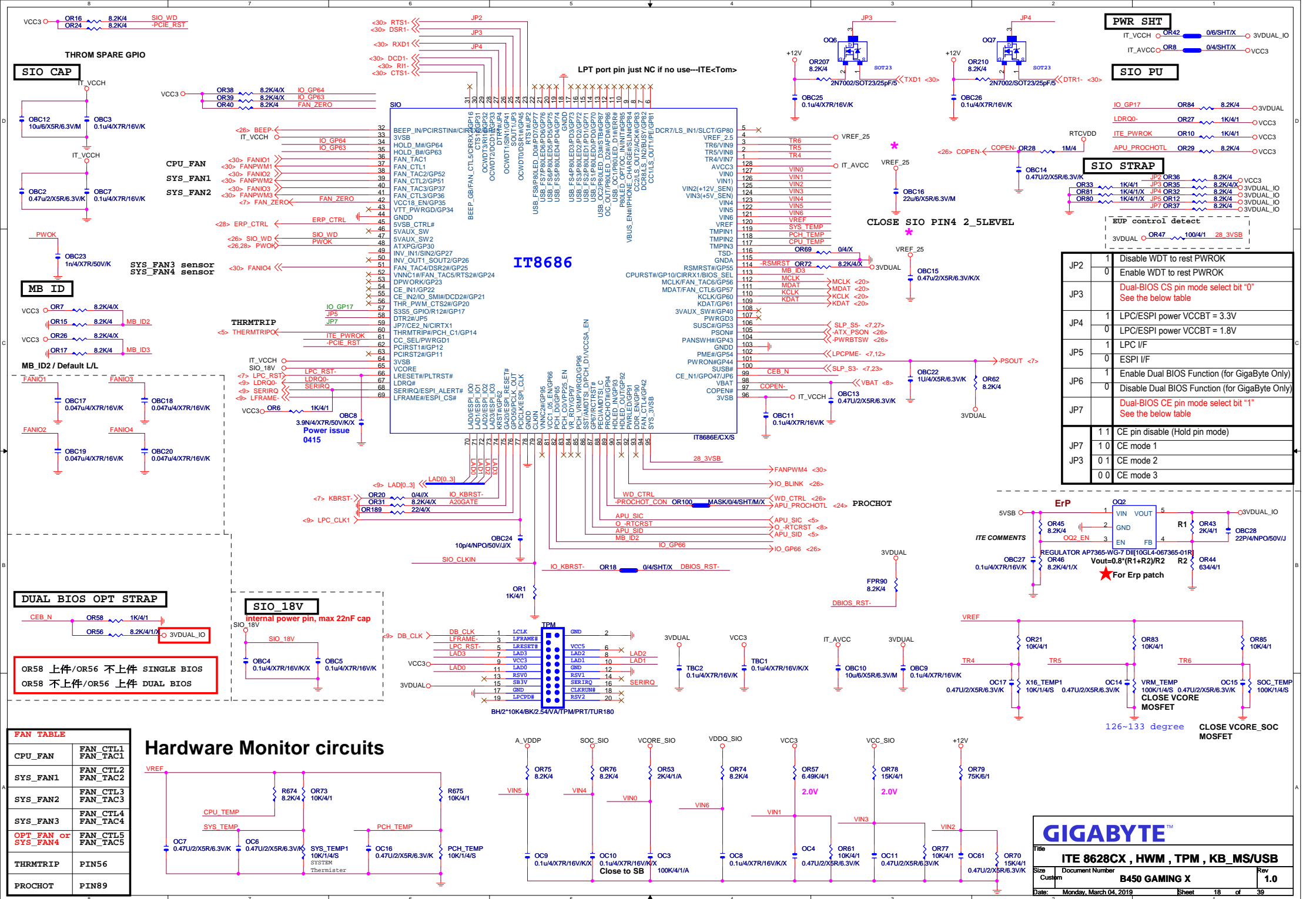


平躺式 DVI-D

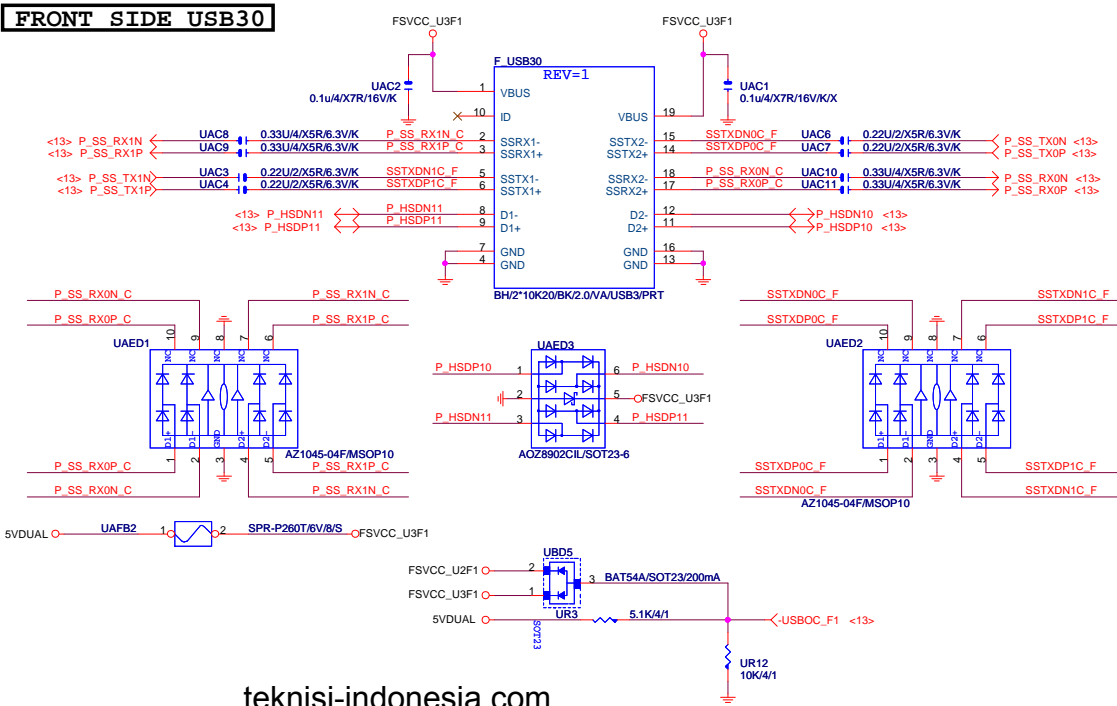


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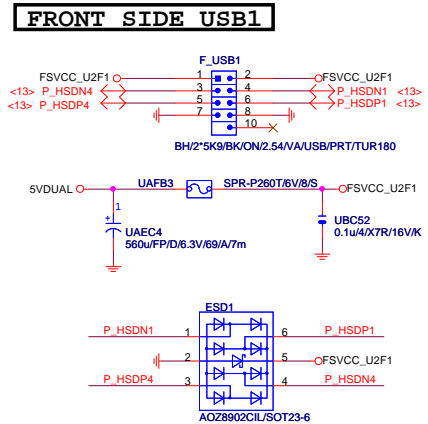
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HDMI 2.0		
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FRONT SIDE USB30

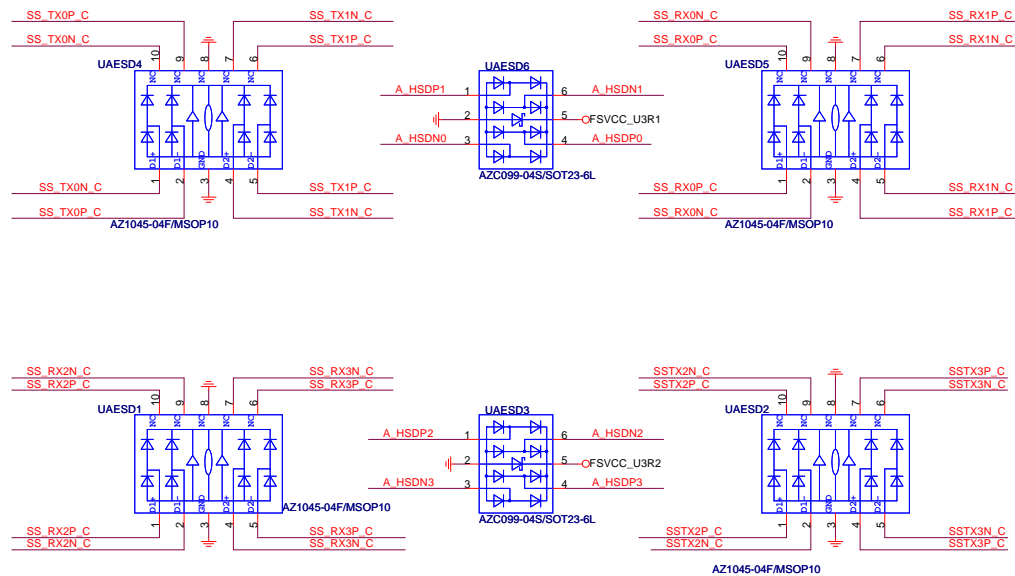
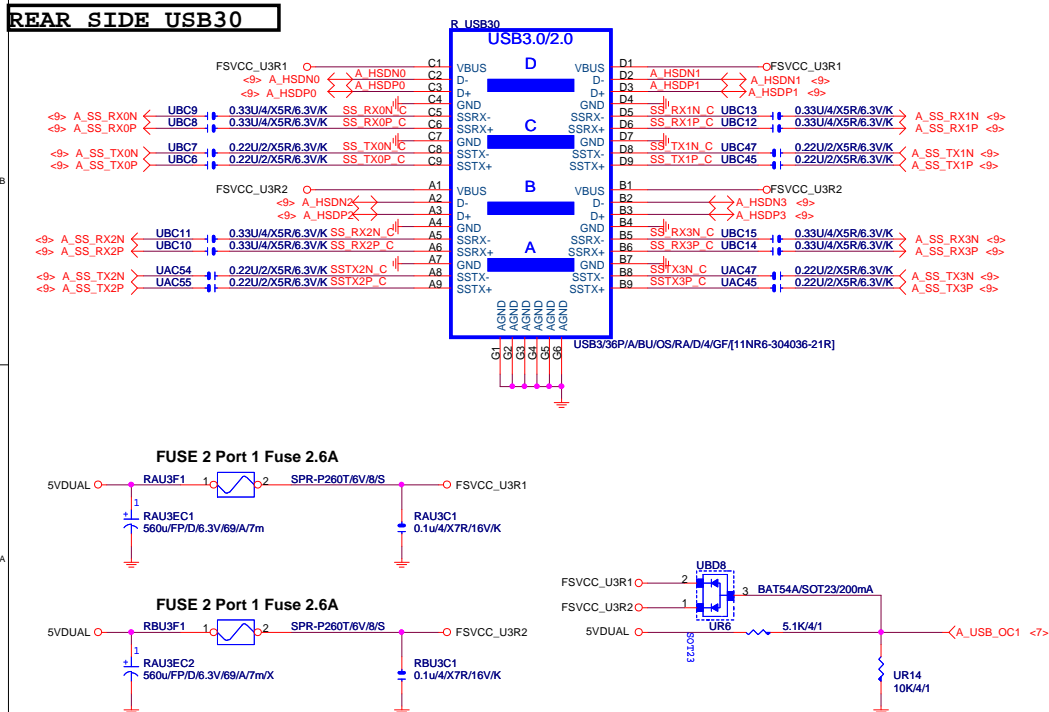


FRONT SIDE USB1



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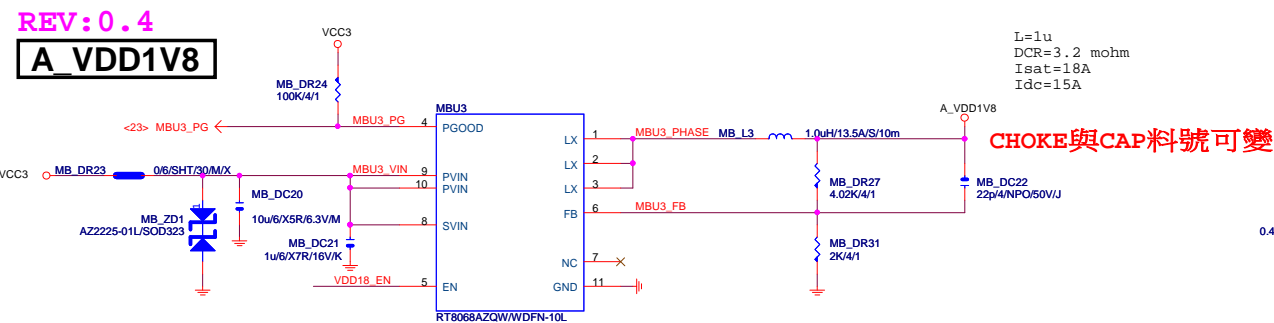
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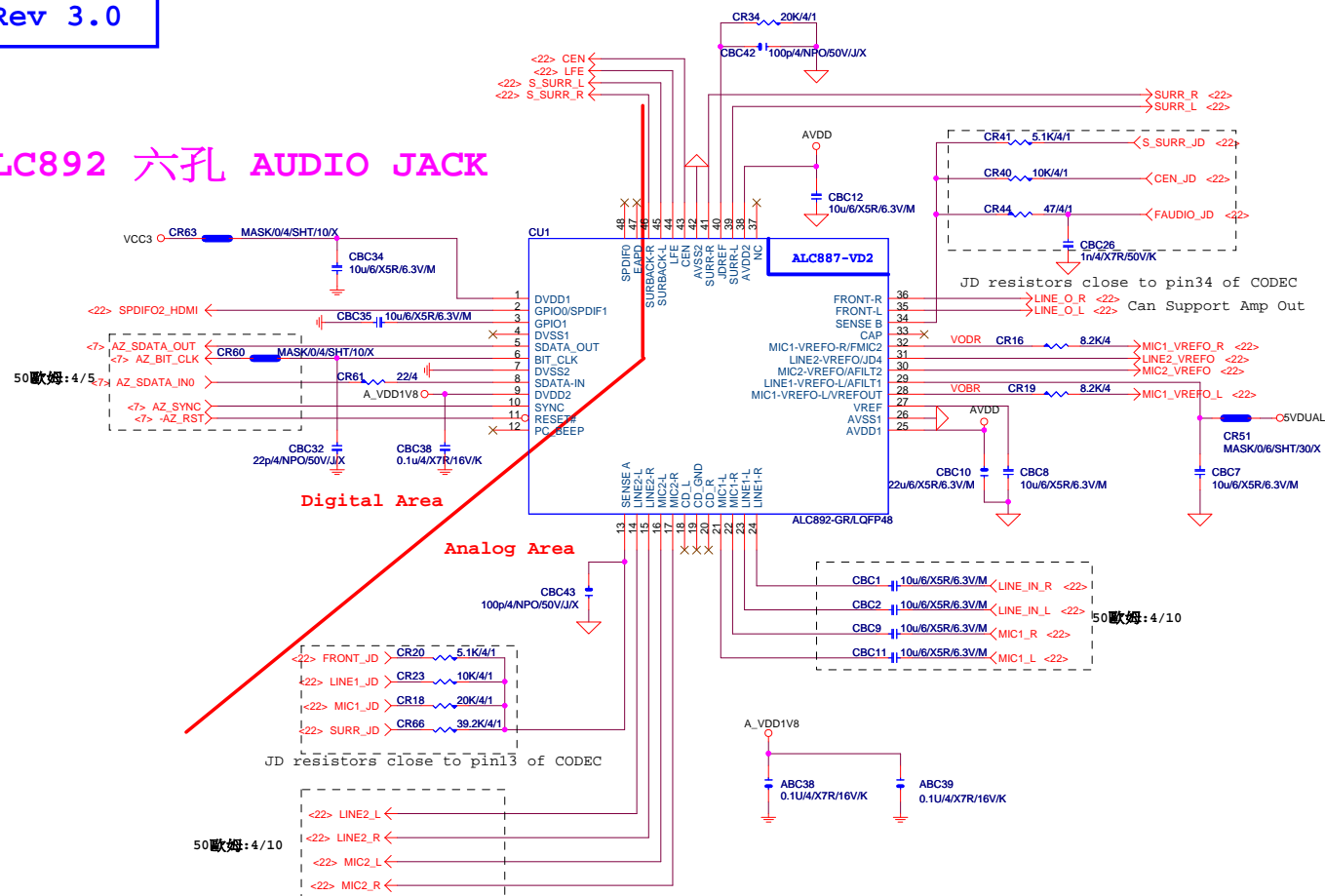
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Title	F_USB, R_USB CONN
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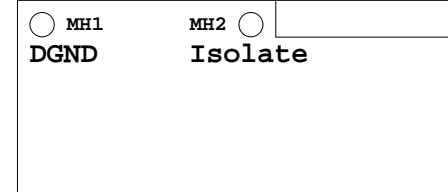


ALC892 六孔 AUDIO JACK



LAYOUT注意:螺絲孔下GND方式

1. MH1空間夠,下DGND
空間不夠,才改為Isolate
2. MH2一律改為Isolate
3. Codec下方,第二層必須參考GND



LAYOUT注意:要加

GND切割線

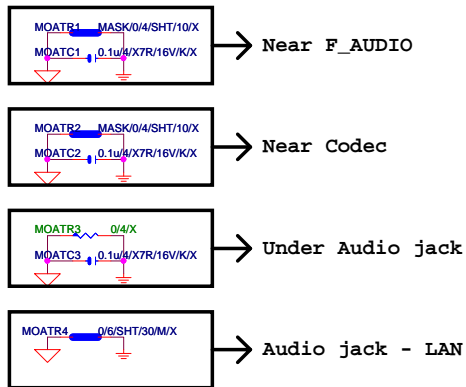
音效區域印刷



- BOM OPTION :
1. Chemicon音效電容
 2. 金屬外罩 Reserve (LAYOUT上件與否,依照各Model spec)
 3. LED Reserve (上件與否和LED顏色,依照各Model spec)

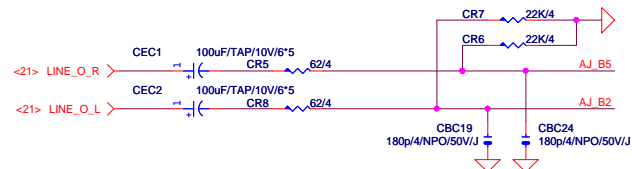
GIGABYTE™			
Title			
ALC1150 CODEC			
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Rev 3.0

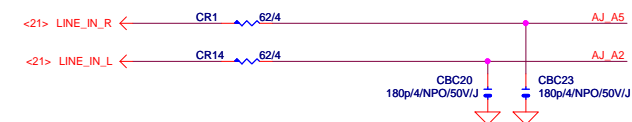


*量産前, 0ohm改short pad

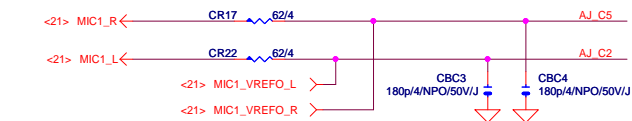
LINE-OUT



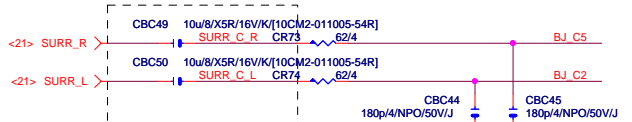
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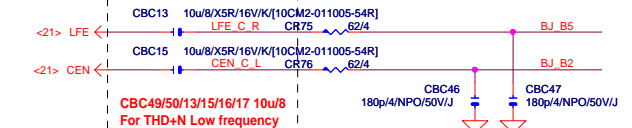
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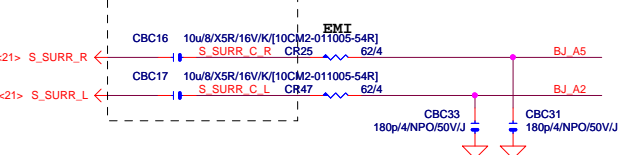
SURROUND



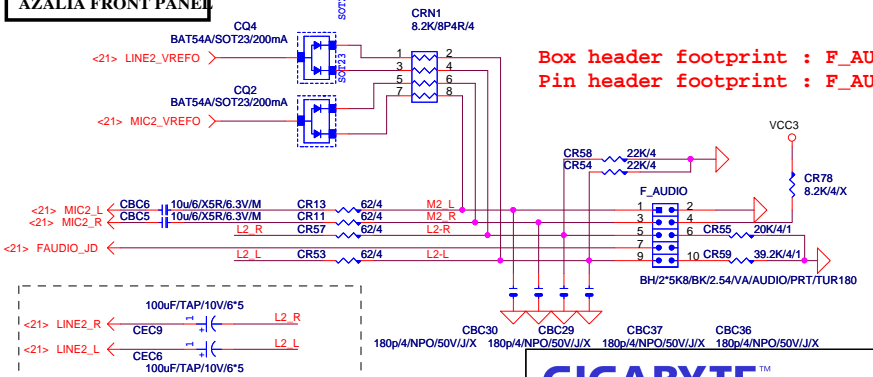
CEN/LFE



SURR BACK

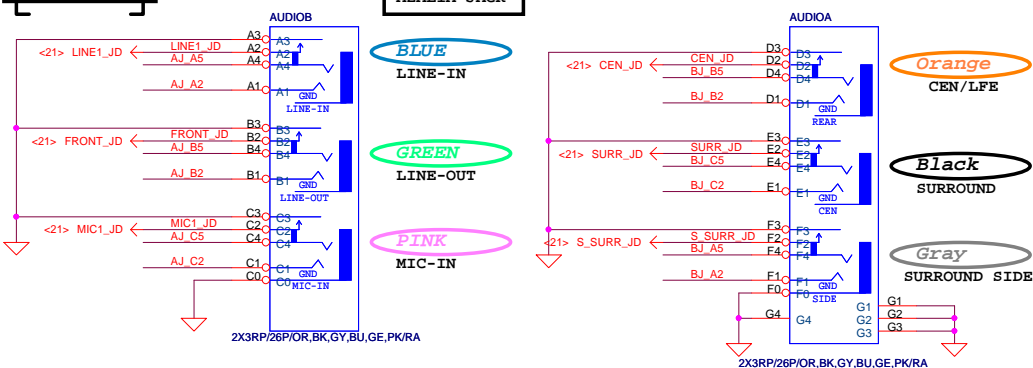
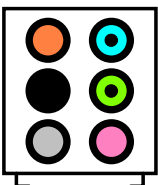


AZALIA FRONT PANEL



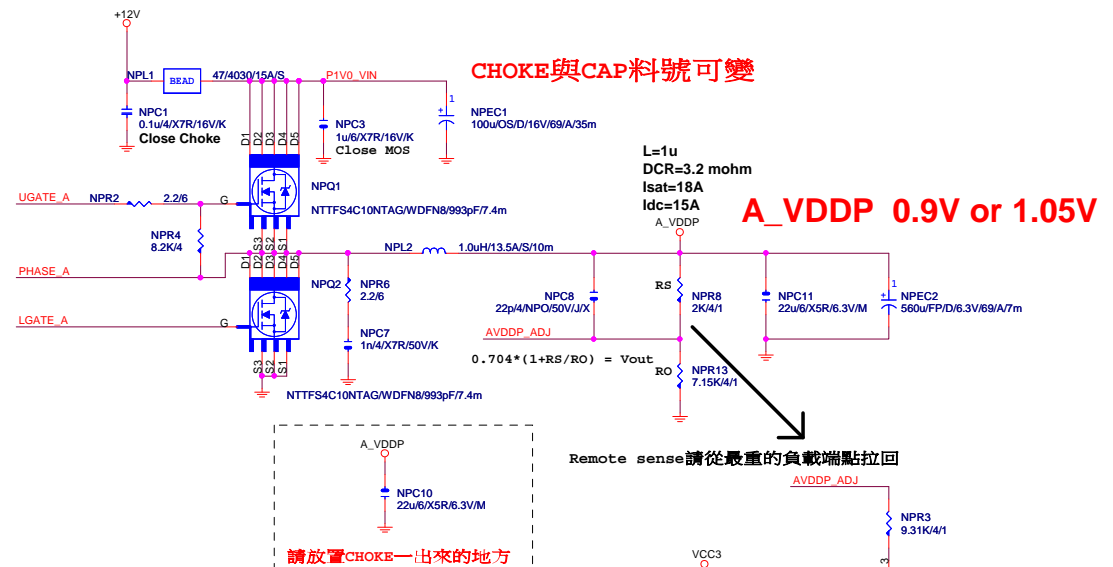
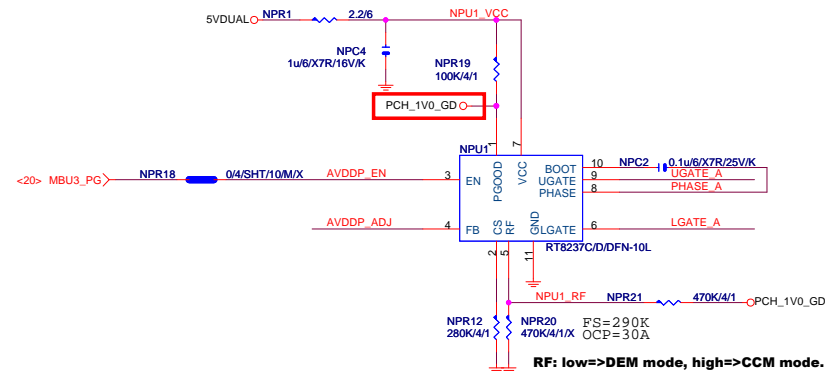
Box header footprint : F_AUDIO
Pin header footprint : F_AUDIO_S

AZALIA JACK

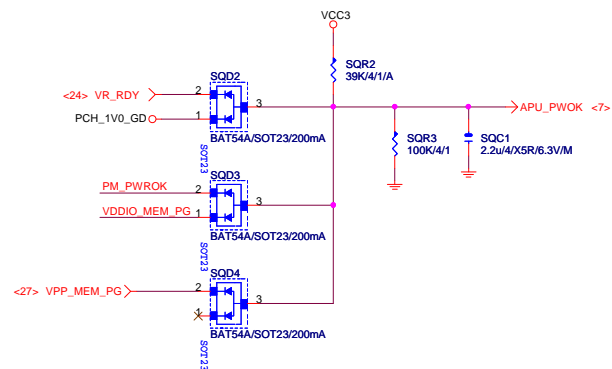
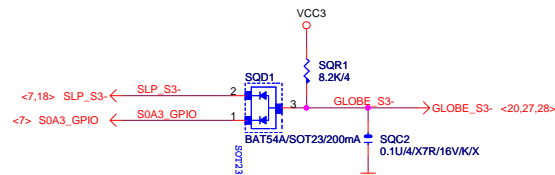


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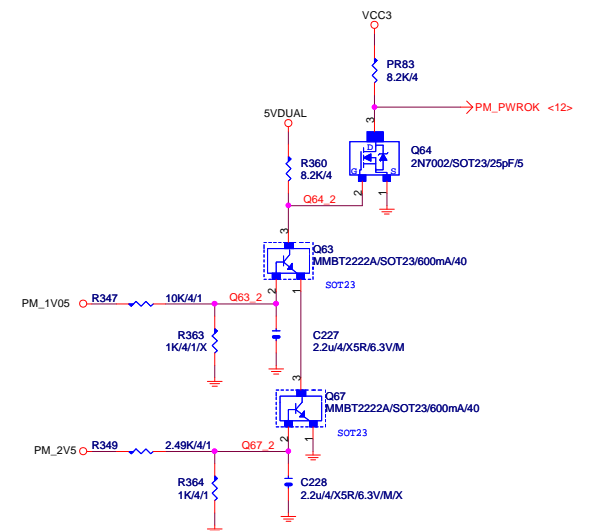
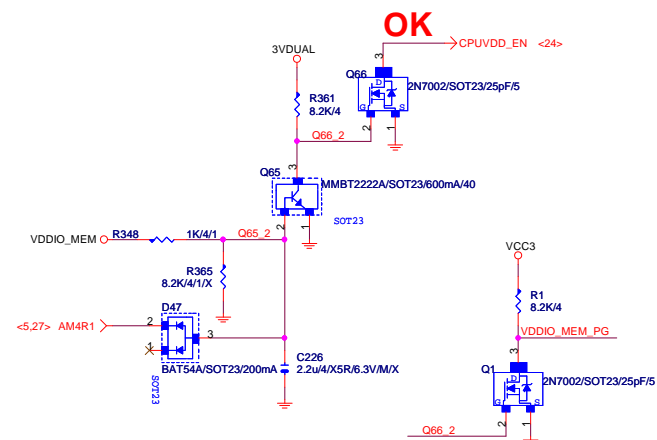
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AUDIO JACK		
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CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

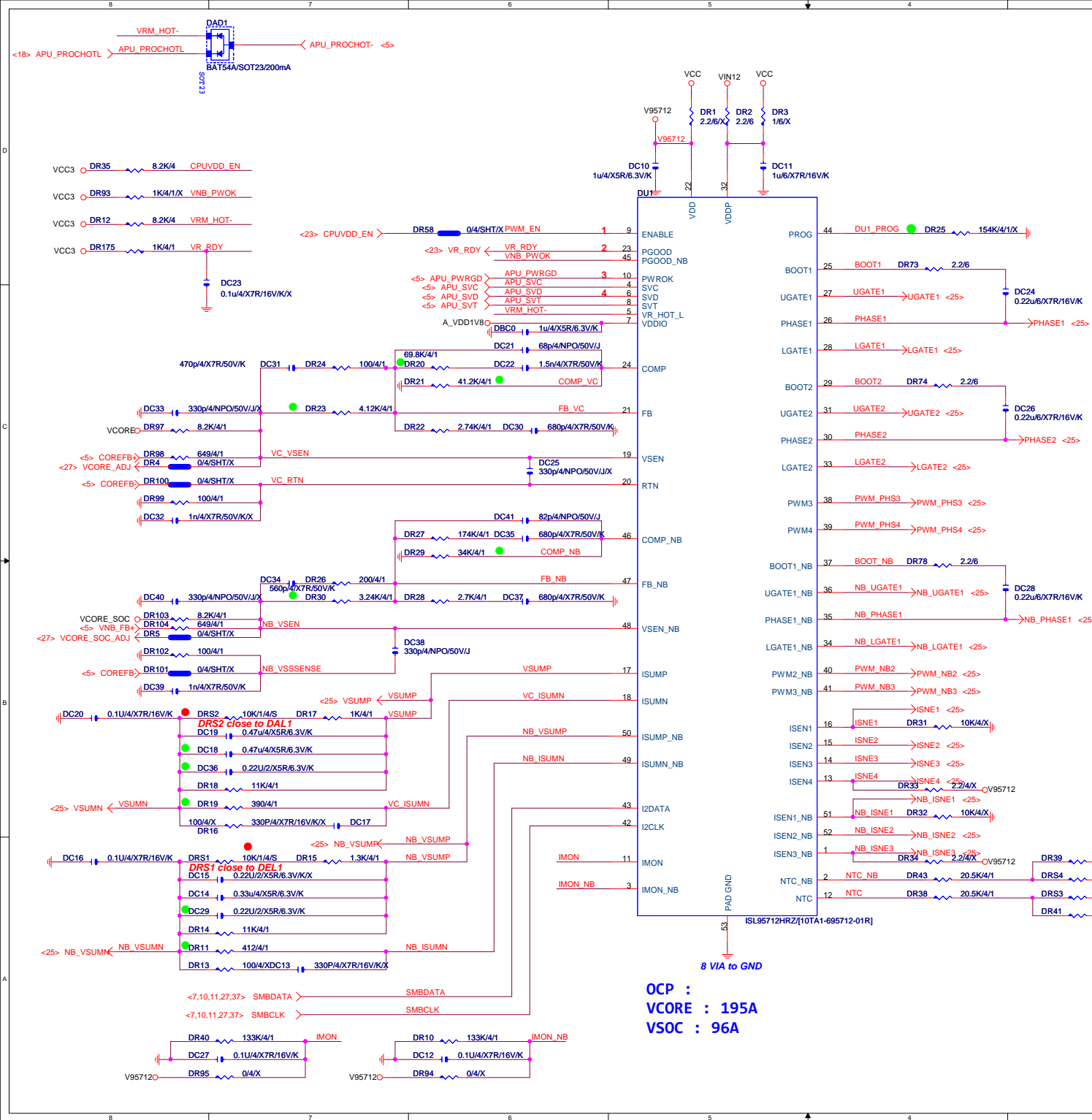


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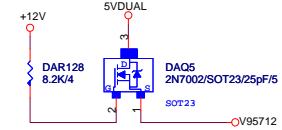


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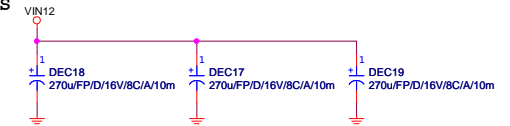
POWER SEQUENCE		
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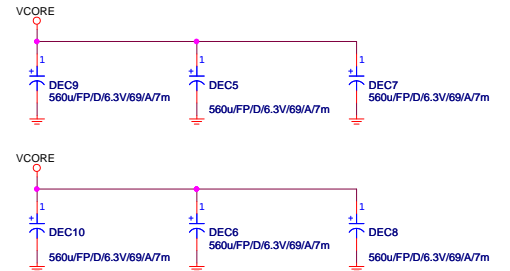
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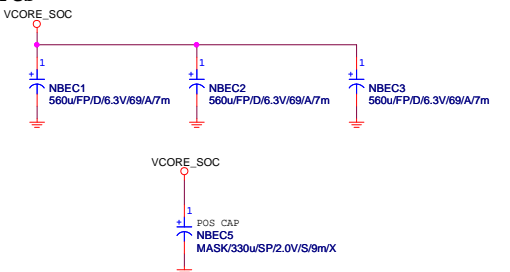
VIN * 3PCS



VCORE * 6 PCS



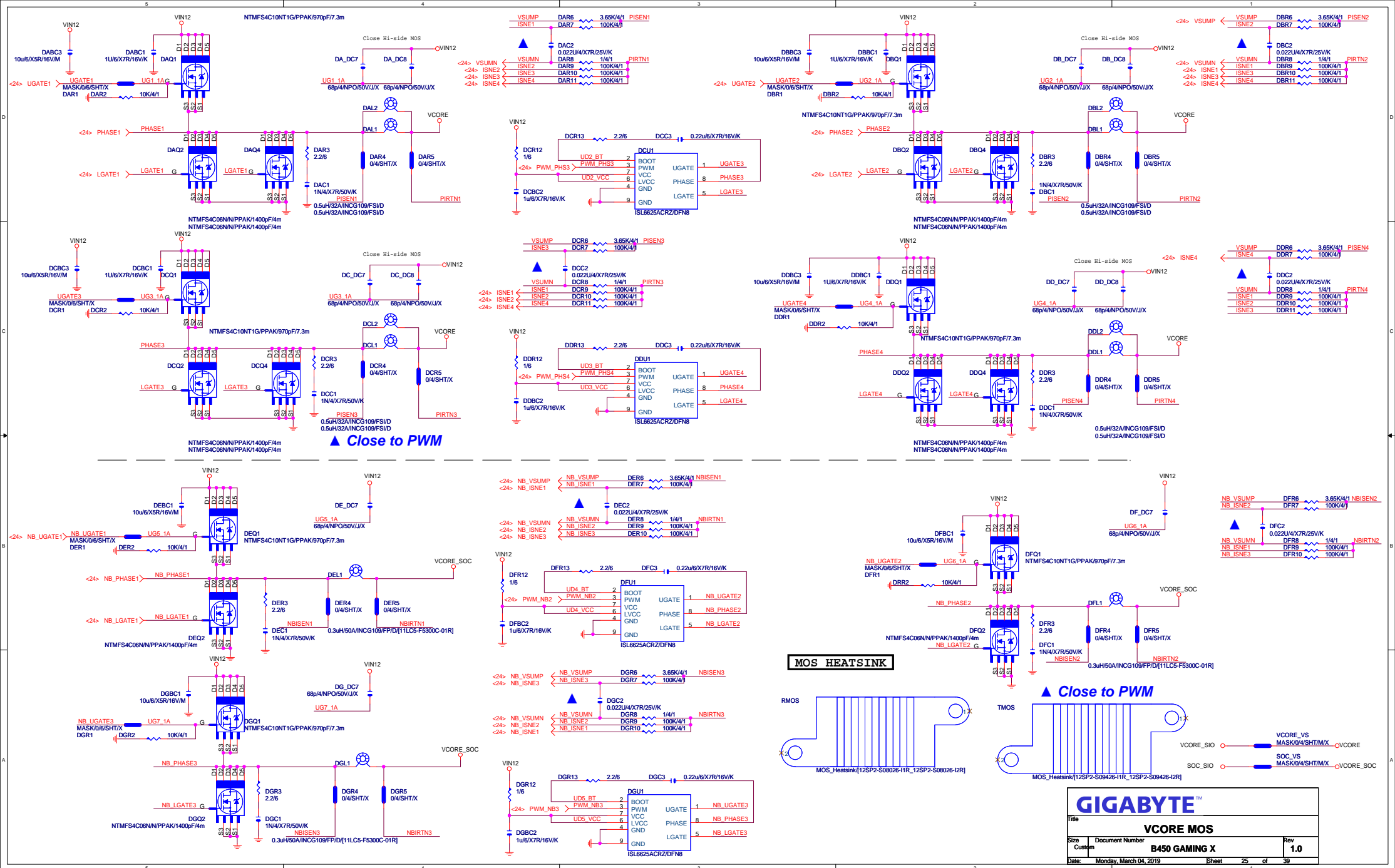
VSOC * 4 PCS

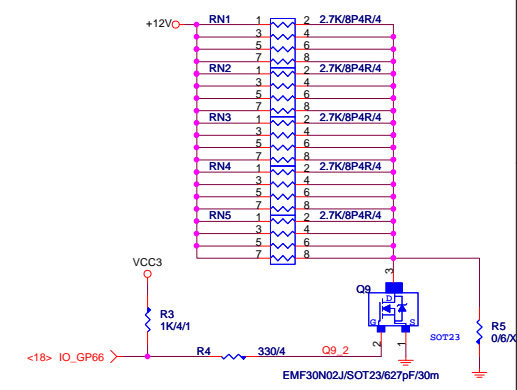
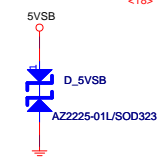
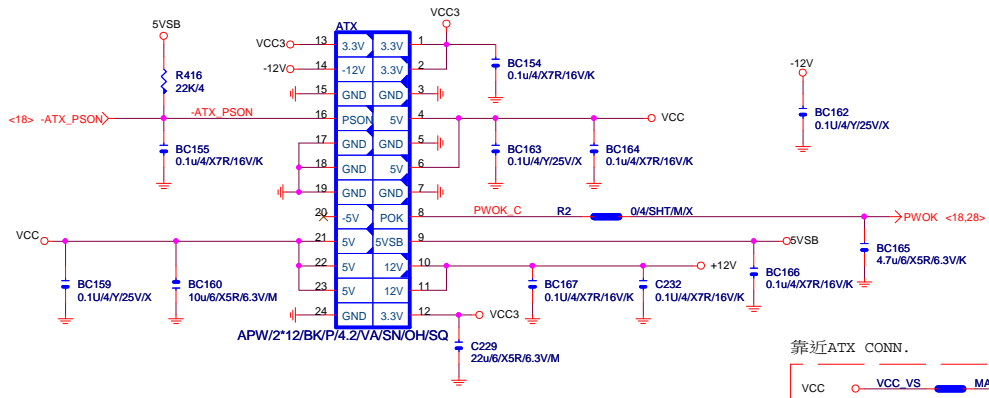
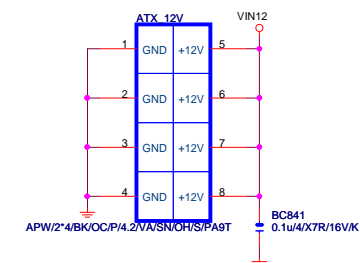
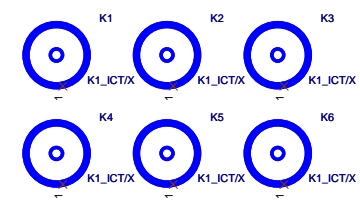
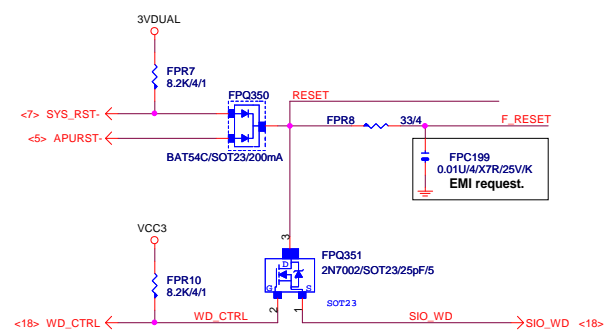


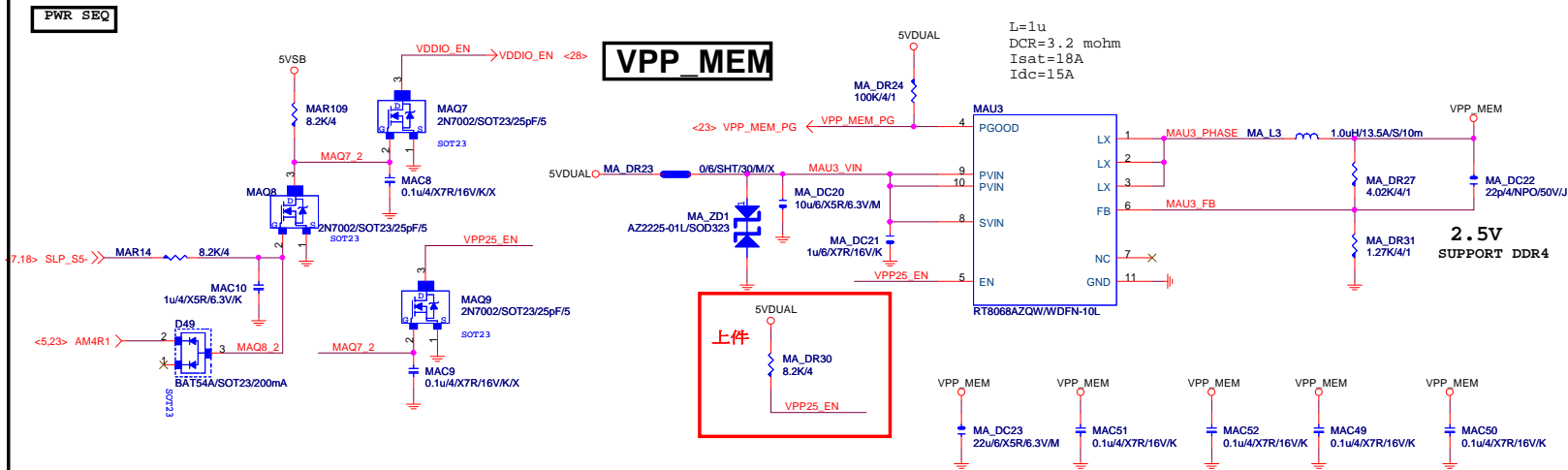
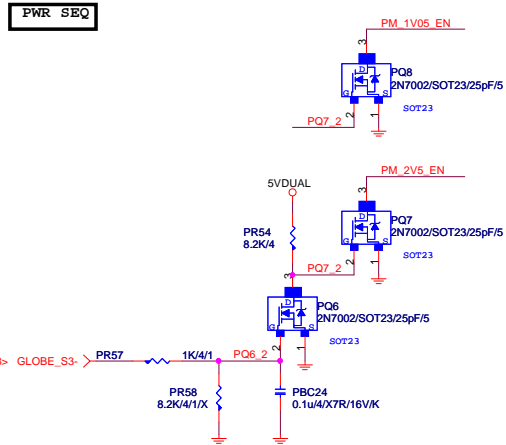
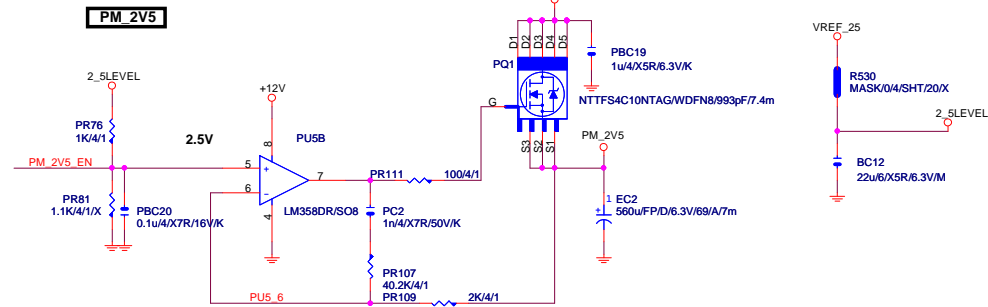
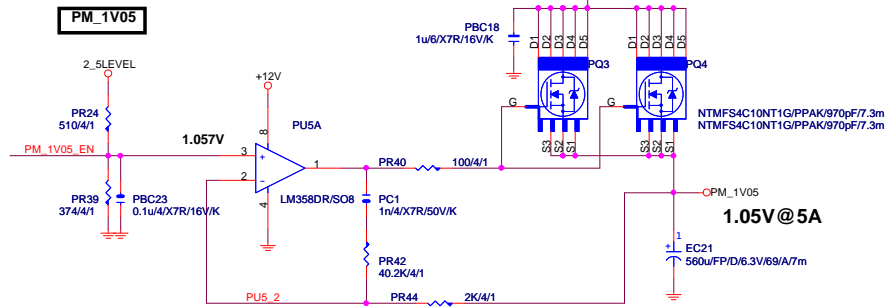
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Title
VCORE (PWM ISL6277+6609A)

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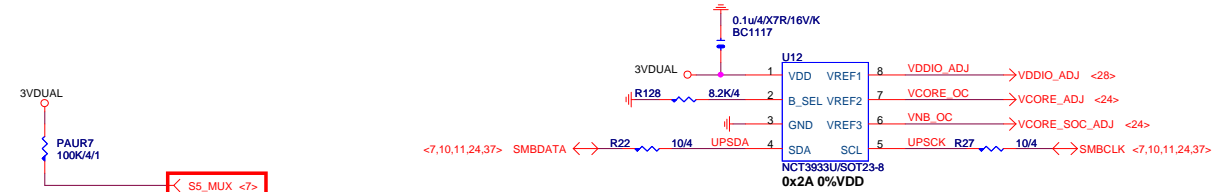




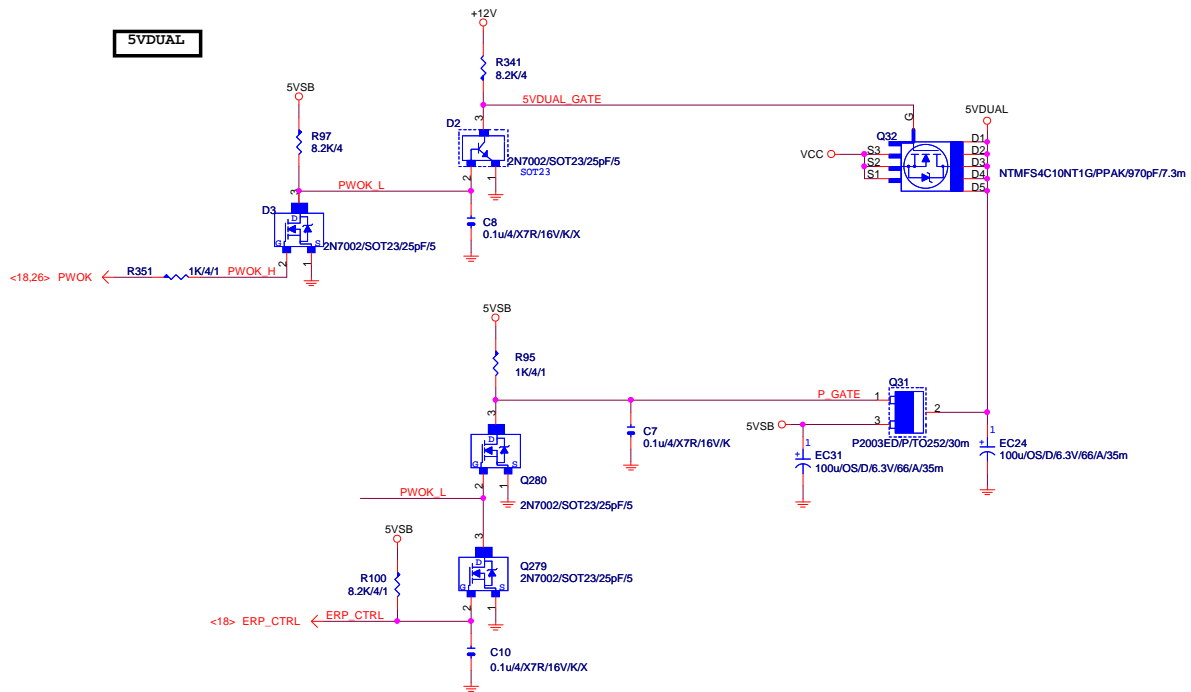
VDDCR SOC S5

S5_MUX: S0-->High, S5-->Low
H: VDDCR_SOC_S5 will track VCORE_SOC.
L: If VCORE_SOC < 0.775V (OR 0.85V) , VDDCR_SOC_S5=0.775V.
If VCORE_SOC>=0.775V (OR 0.85V) , VDDCR_SOC_S5 will trace VCORE_SOC.

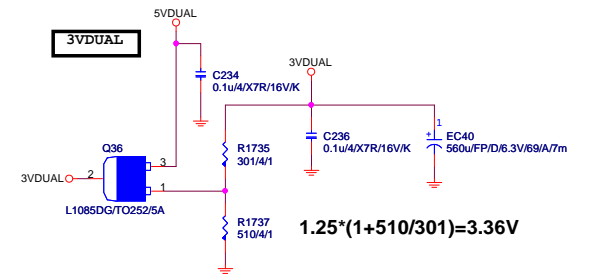
AM4 S5: 0.775V, 200mA,
S0:VAR, 900mA.



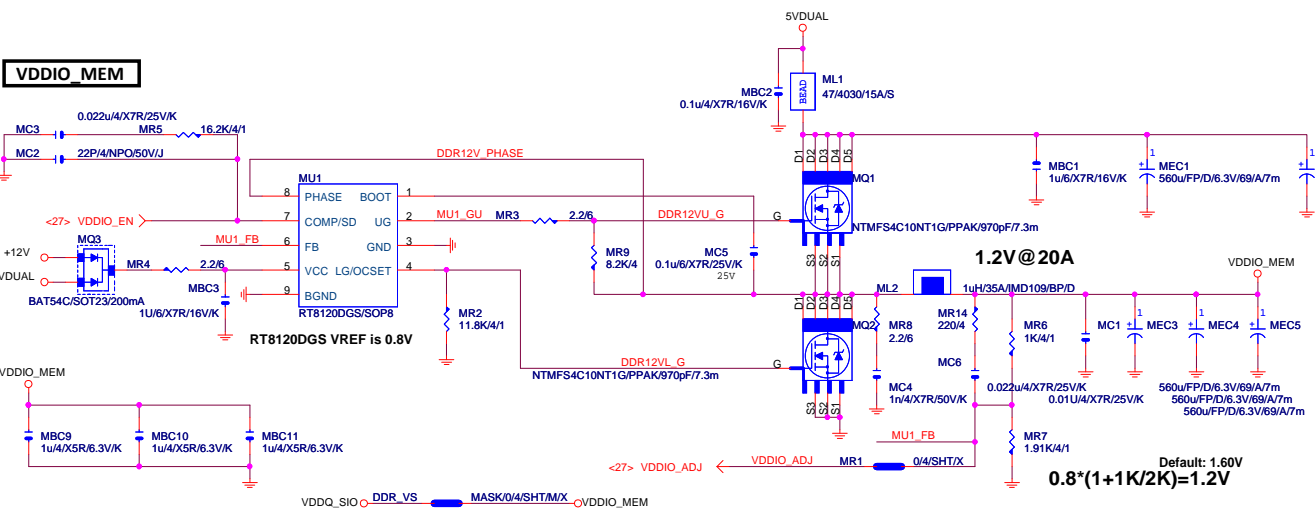
5VDUAL



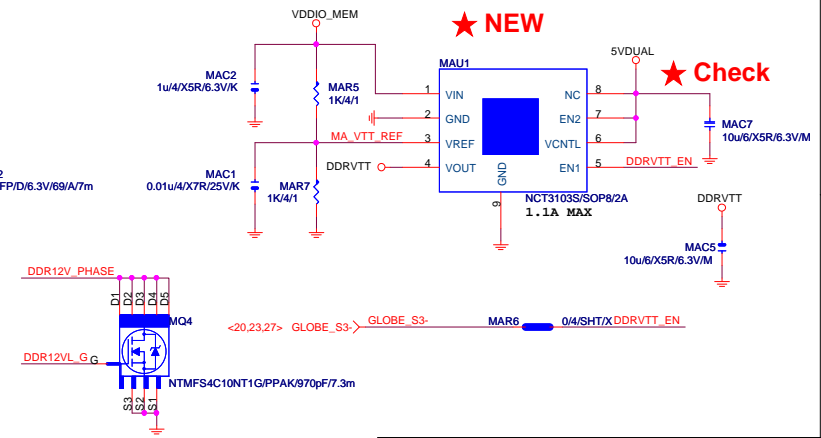
3VDUAL



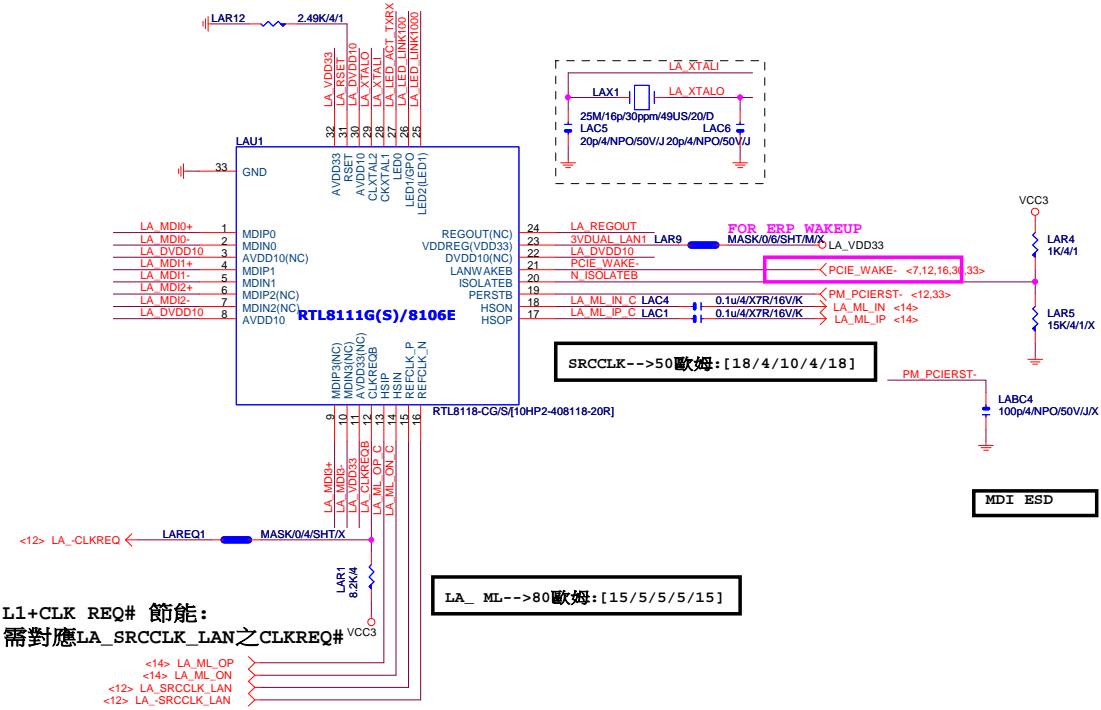
VDDIO_MEM



DDRVTT

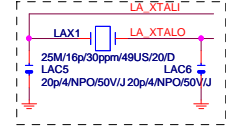


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DDR PWR, 5VDUAL, 3VDUAL		
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L1+CLK REQ# 節能:
需對應LA_SRCCLK LAN之CLKREQ#
<14> LA_ML_ON
<14> LA_ML_ON
<12> LA_SRCCLK_LAN
<12> LA_SRCCLK_LAN

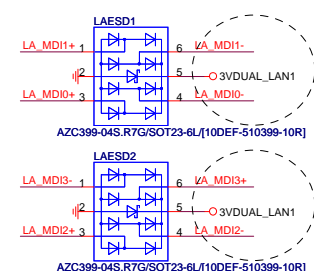
LA_ML-->80歐姆:[15/5/5/5/15]



FOR ERP WAKEUP
MASK/0/6/SHT/M/X

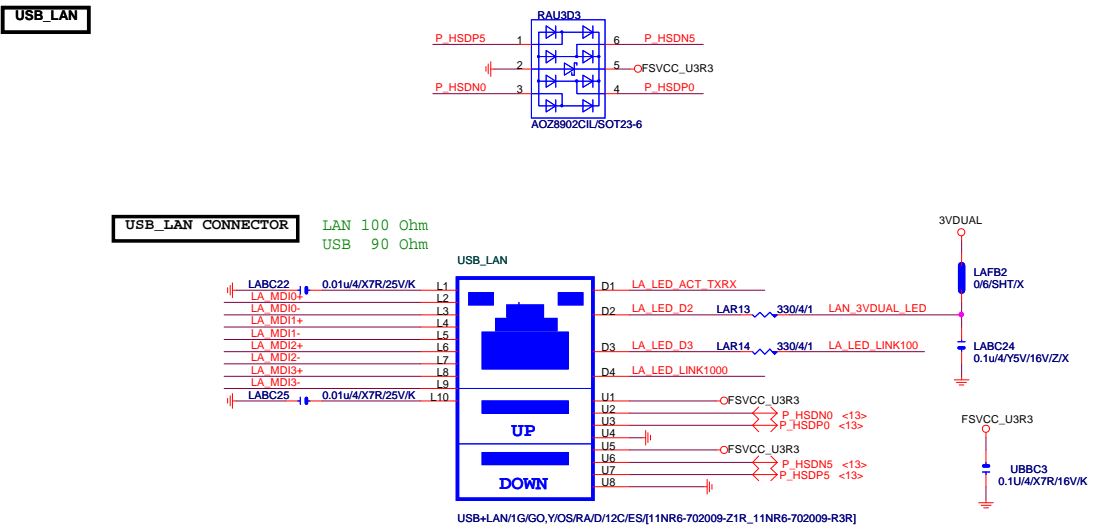
SRCLK-->50歐姆:[18/4/10/4/18]

MDI ESD

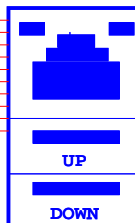


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USB_LAN

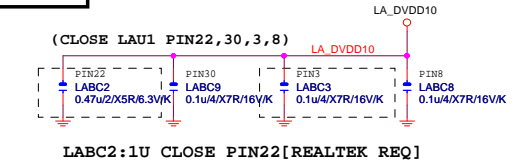


USB_LAN CONNECTOR
LAN 100 Ohm
USB 90 Ohm



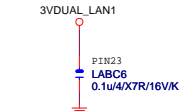
USB+LAN1G/GQ, I/O/S/RAD/12C/ES/[11NR6-702009-Z1R_11NR6-702009-R3R]

LAN POWER

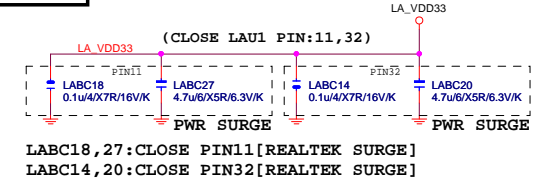


LAN POWER

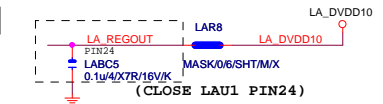
note: lan power連接及電流



LAN POWER



LAN POWER



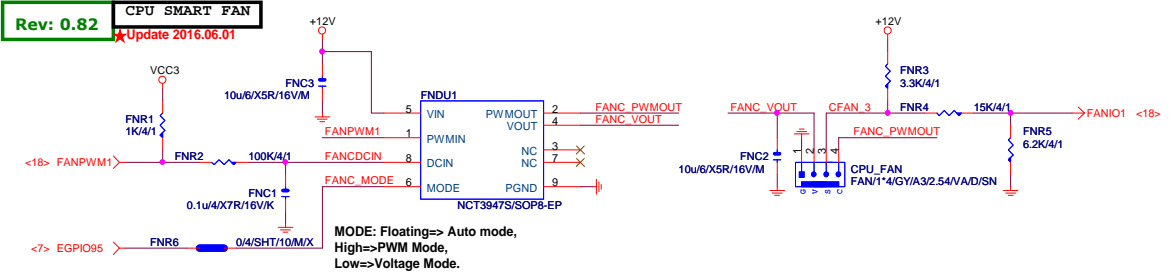
LAN POWER

note: lan power連接及電流

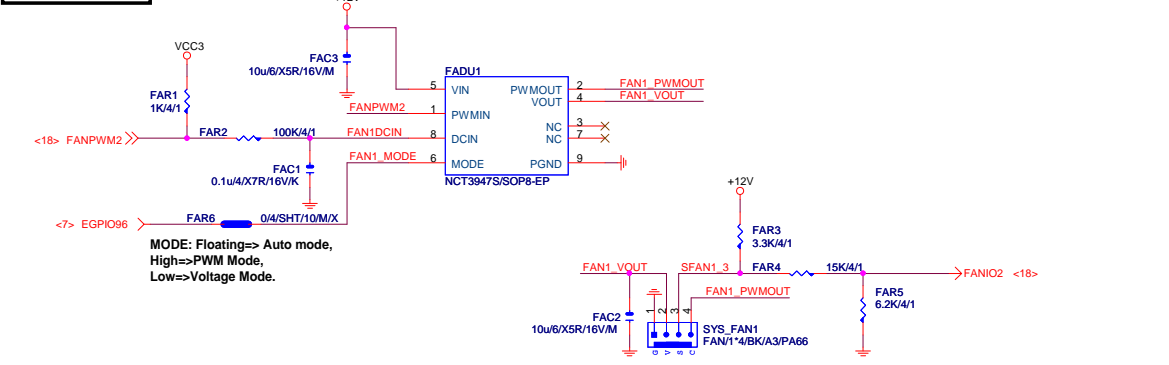
可變 3VDUAL_LAN1 - LAPW1 MASK/0/4/SHT/M/X 3VDUAL

EMI SHORT PAD

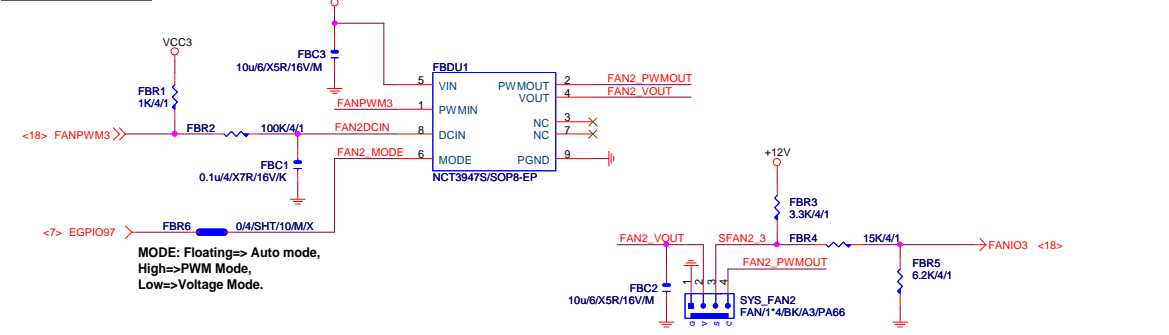
PS:視EMI需求



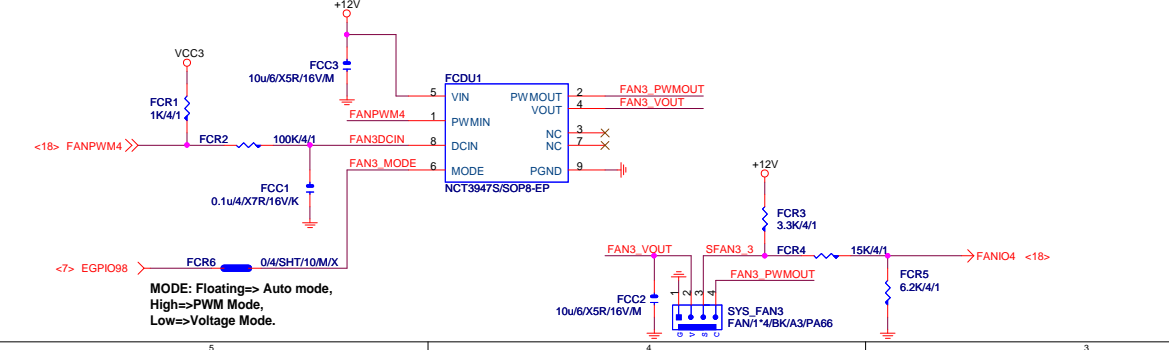
SYSTEM FAN1



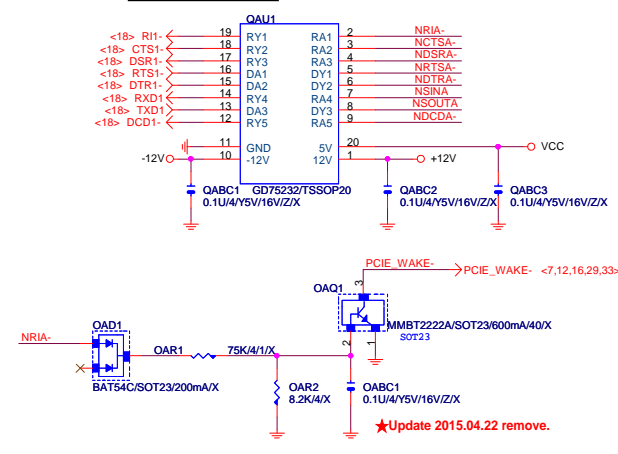
SYSTEM FAN2



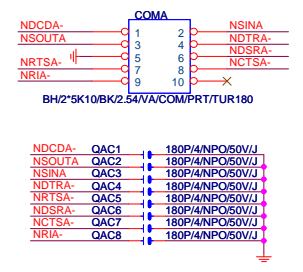
SYSTEM FAN3



COM PORT

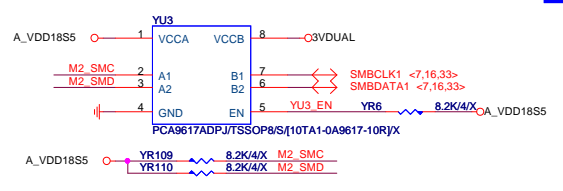
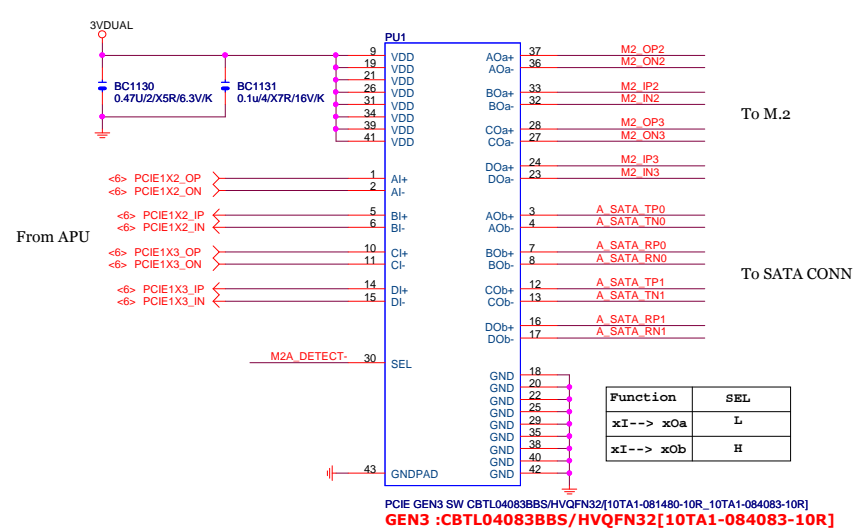
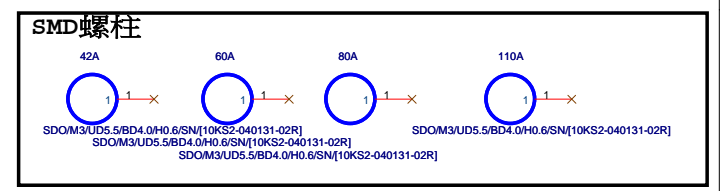
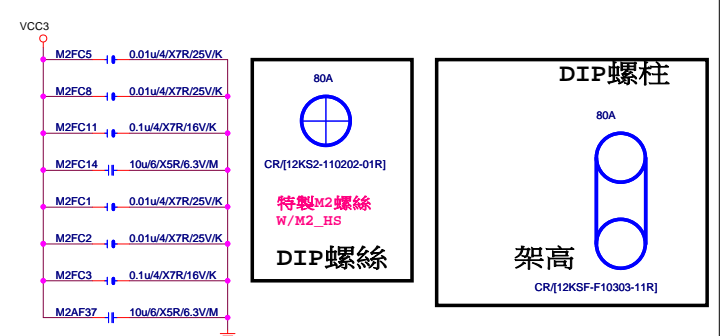


COMA

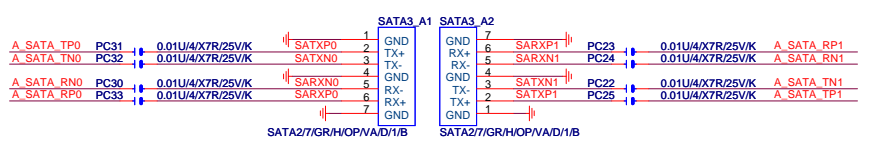


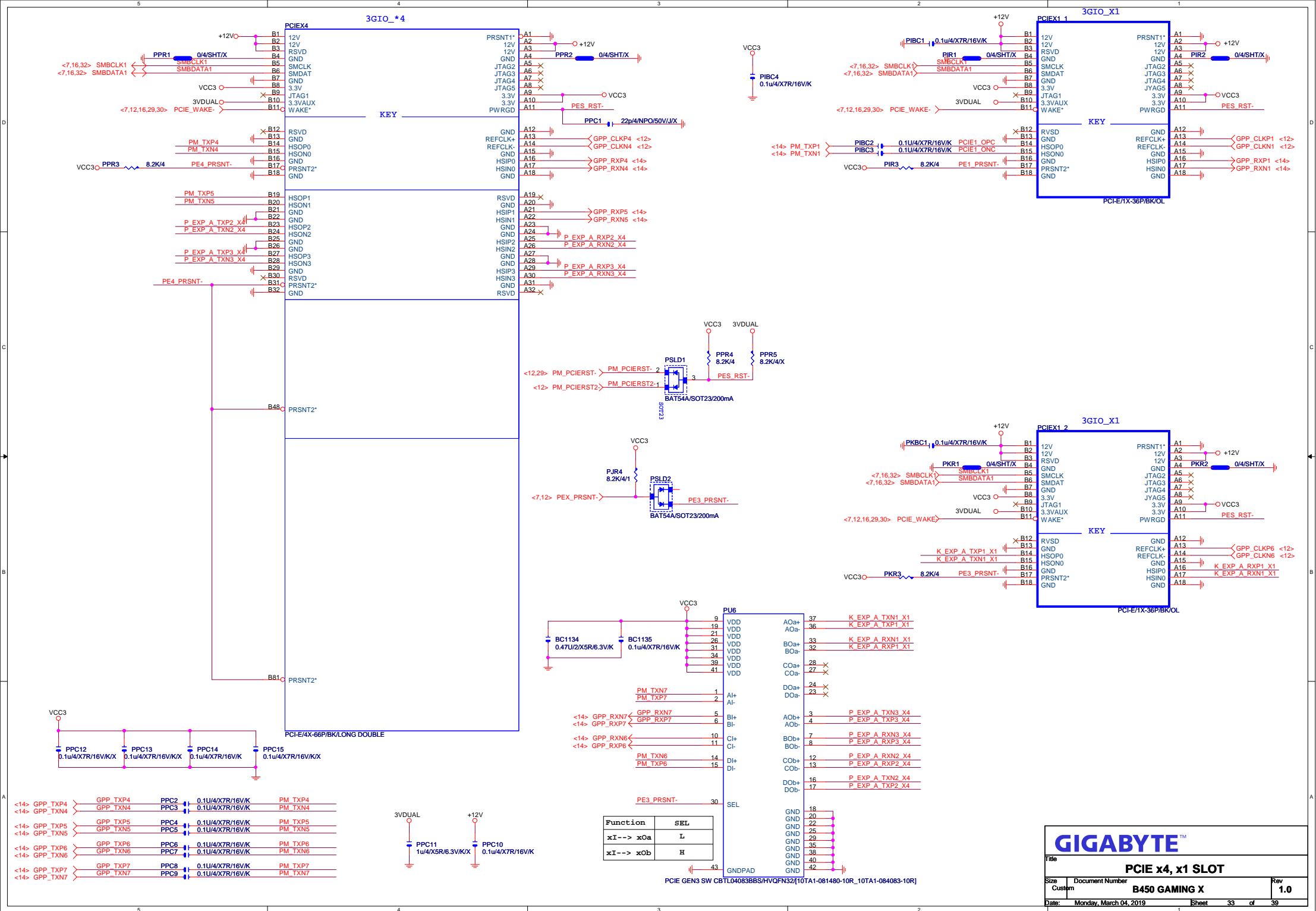
5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	

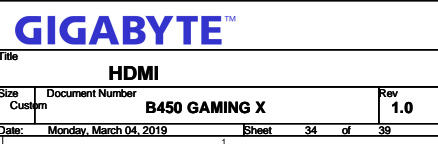
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Title DP to VGA			
Size Custom	Document Number B450 GAMING X		Rev 1.0
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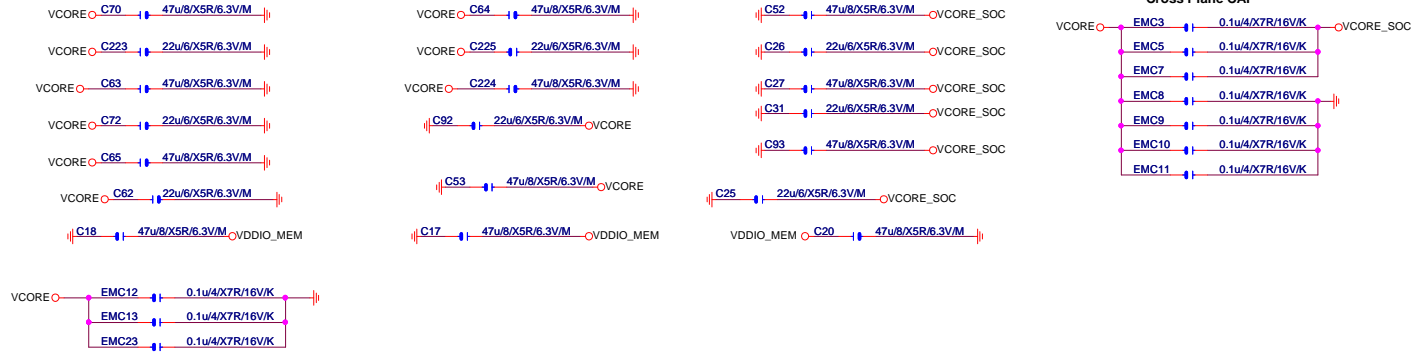
Function	SEL
xI--> x0a	L
xI--> x0b	H







CPU TOP CAVITY



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HDMI			
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